Amendments to the Specification:

Please replace the paragraph beginning at page 4, line 19 and ending at page 4, line 31 with the following amended paragraph:

-- More particularly, FIG. 2 is a block diagram illustrating in greater detail the lookup system of FIG. 1. As shown, the system 105 includes a buffer 206 for receiving incoming data packets from the input port 104, and a routing controller 208 for routing the packets to the appropriate output port(s) 112. Also included is a lookup table including DRAM cache 204 [[202]] and SRAM cache 202 [[204]] according to embodiments of the present invention. In operation, data packets are received from the input port(s) into the buffer 206. Their headers, which may be of a known format, are then read and by the routing controller 208. The routing controller 208 accesses the lookup table to determine where the packets are to be routed. The SRAM 202 is used to store a first search level of destination addresses. Once the first search level in SRAM 202 has been exhausted, the search moves to the DRAM portion 204. Once the search is completed, the packets are then routed appropriately. --